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**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

10

Application Number

10/665,757

Filing Date

September 19, 2003

First Named Inventor

Glenn J. Leedy

Art Unit

2822

Examiner Name

Pamela E. Perkins

Attorney Docket Number

ELM-1 Cont. 9

ENCLOSURES (Check all that apply)

- | | | |
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| <input type="checkbox"/> Fee Transmittal Form (in duplicate)
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RemarksThe Director is hereby authorized to charge any fee(s) that may be due under 37 CFR 1.16 or 1.17 to Deposit Account No. 06-1075. A duplicate copy of this letter is enclosed.**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm Name

Customer No. 1473

Signature

Printed name

Jeffrey C. Aldridge

Date

November 13, 2007

Reg. No.

51,390

CERTIFICATE OF TRANSMISSION/Express Mail No. EM 014770295 US

I hereby certify that this correspondence is are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to Hon. Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Signature

Typed or printed name

Sarah Schlie

Date

November 13, 2007

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Express Mail No. EM 014770295 US

PATENTS
ELM-1 Cont. 9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant : Glenn J. Leedy
Application No.: 10/665,757 Confirmation No.: 6828
Filed : September 19, 2003
For : METHOD OF MAKING AN INTEGRATED CIRCUIT
Group Art Unit : 2822
Examiner : Pamela E. Perkins

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicant wishes to call the attention of the Examiner to the
following documents:

U.S. PATENT DOCUMENTS

3,430,835	Patzer et al.	03/04/1969
4,196,232	Schnable et al.	04/01/1980
5,615,163	Sakui et al.	03/25/1997
5,786,629	Faris	07/28/1998
5,787,445	Daberkó	07/28/1998
6,563,224	Leedy	05/13/2003

11/19/2007 SSITHIB1 00000003 061075 10665757

01 FC:1806

180.00 DA

The Information Disclosure Statement filed herewith is submitted after the mailing date of a Final Office Action, a Notice of Allowance, or an Office Action that otherwise closes prosecution. Accordingly, a \$180.00 fee is due pursuant to 37 C.F.R. § 1.17(p). The director is hereby authorized to charge the \$180.00 fee, and any additional fees that are due, to Deposit Account No. 06-1075.

Respectfully submitted,



Jeffrey C. Aldridge
Reg. No. 51,390
Agent for Applicant
ROPES & GRAY LLP
Customer No. 1473
1211 Avenue of the Americas
New York, New York 10036-8704
Tel.: (212) 596-9000
Fax: (212) 596-9090

<u>No.</u>	<u>FOREIGN DOCUMENTS</u>		
1	JP 01-157561 A	Japan	06/20/1989
2	JP 02-037655	Japan	02/07/1990
3	JP 03-127816	Japan	05/30/1991
4	JP 03-174715	Japan	07/29/1991
5	JP 05-283607 A	Japan	10/29/1993
6	JP 08-504060 A	Japan	04/30/1996
7	JP 62-272556 A	Japan	11/26/1987
8	JP 61-30059 A	Japan	02/12/1986
9	JP 04-042957	Japan	02/13/1992
10	JP 05-109977 A	Japan	04/30/1993
11	JP 09-152979 A	Japan	06/10/1997
12	JP 10-107065	Japan	04/24/1998
13	JP 10-209371 A	Japan	08/08/1998

<u>No.</u>	<u>NON-PATENT DOCUMENTS</u>
1	S. Wolf, Silicon Processing, 1990, Lattice Press, Volume 2, Page 111.
2	Wolf, Stanley and Richard N. Tauber; Silicon Procesing For the VLSI Era, Volume 1: Process Technology; Sunset Beach, CA: Lattice Press, 1986, pp. 191-194.
3	S. Wolf, Silicon Processing For the VLSI Era, 1990, Lattice Press, Volume 2, page 191.

The aforementioned U.S. Patent Documents, which are listed on the accompanying Form PTO/SB/08 (submitted in duplicate), fall under 37 C.F.R. § 1.98(a)(2)(ii) for which the requirement to provide copies is waived. Accordingly, no copies of the aforementioned U.S. Patent Documents are provided. Copies of the aforementioned foreign documents and non-patent documents are being provided herewith.

U.S. Patent No. 3,430,835 was cited in an Office Action dated October 9, 2007 in co-pending commonly assigned U.S. Patent Application No. 10/971,341. U.S. Patent No.

4,196,232 was cited in an Office Action dated April 10, 2007 in co-pending commonly assigned U.S. Patent Application No. 10/741,647. U.S. Patent No. 6,563,224 was cited in an Office Action dated October 16, 2003 in co-pending commonly assigned U.S. Patent Application No. 10/379,820.

Above-identified foreign documents 1 and 5-13 were cited in an Office Action dated February 1, 2007 in Japanese Patent Application No. 10-543031, which is the Japanese counterpart of U.S. Patent Application No. 08/835,190, now U.S. Patent No. 5,915,167. Foreign document 2 was cited in an Office Action dated May 17, 2005 in Japanese Patent Application No. 2003-411658, now Japanese Patent No. 3816483, which is the Japanese counterpart of U.S. Patent Application No. 09/027,959, now abandoned. Foreign documents 3 and 4 were cited in an Office Action dated October 8, 2004 in Japanese Patent Application No. 2003-411658, now Japanese Patent No. 3816483, which is the Japanese counterpart of U.S. Patent Application No. 09/027,959, now abandoned.

Above-identified non-patent document 1 was cited in an Office Action dated June 1, 2007 in co-pending commonly assigned U.S. Patent Application 10/379,820. Non-patent document 2 was cited in an Office Action dated January 26, 2006 in co-pending commonly assigned U.S. Patent Application No. 10/741,647. Non-patent document 3 was cited in an Office Action dated April 20, 2006 in co-pending commonly assigned U.S. Patent Application No. 10/379,820.

It is respectfully requested that these references be: (1) fully considered by the Patent and Trademark Office

during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-SB/08A, as considered and initialed by the Examiner, be returned with the next communication.

The Examiner is advised that the following applications, listed in the table below, contain subject matter that may be related to the pending claims in the present application. In particular, applicant would like to draw the Examiner's attention to the fact that substantive examination may have occurred in these applications, and applicant invites the Examiner to review any Office Actions that have issued or will issue in these cases. At the Examiner's request, we will provide copies of any Office Actions and/or responses to Office Actions that have issued in these applications. By bringing these applications to the Examiner's attention, applicant does not waive the confidentiality provisions of 35 U.S.C. 122.

<u>Application No.</u>	<u>Filing Date</u>
10/143,200	05/13/02
10/222,816	08/19/02
10/379,820	03/03/03
10/460,483	06/11/03
10/672,961	09/26/03
10/700,429	11/03/03
10/741,602	12/18/03
10/741,647	12/18/03
10/742,282	12/19/03
10/971,341	10/22/04
11/042,581	01/24/05